adding the first sum vector and the first carry vector to generate a pixel average value.

9. (Amended) Apparatus comprising:

a compressor stage including a plurality of compressors, each compressor operative to compress a plurality of operands and a rounding vector into a first sum vector and a first carry vector and to discard a two least significant bits (LSBs) of said first sum vector and an LSB of the first carry vector; and

a Single-Instruction/Multiple-Data (SIMD) adder operative to add the first sum vector and the first carry vector to generate an average pixel value.

16. (Amended) An article comprising a machine-readable medium include machine readable instructions, the instructions operative to cause a machine to:

compress a plurality of pixel values and a rounding vector into a first sum vector and a first carry vector;

discard a least significant bit of the first carry vector;

discard a two least significant bits of the first sum vector; and

add the first sum vector and the first carry vector to generate a pixel average value.--